REMARKS

Reconsideration of this application, as amended, is respectfully requested.

Claims 1-6, 8-9 and 11-15 are pending. Claims 1-6, 8-9 and 11-15 stand rejected.

In this response, claims 1, 13, and 15 have been amended. No claims have been canceled. No claims have been added. Support for the amendments is found in the specification, the drawings, and in the claims as originally filed. Applicants respectfully submit that the amendments do not add new matter.

REJECTIONS UNDER 35 U.S.C. § 103

Claims 1, 8, 9 and 11 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,060,033 to Takeuchi ("Takeuchi '033").

With respect to claim 1, the Examiner stated the following:

> Regarding the limitation "having recesses,...and a pair of silicon or silicon alloy inwardly concaved source/drain regions of a second conductivity type formed in said recesses", this is a product-by-process limitation that discloses a method of forming source/drain regions that are inwardly concave, however, since the claims are directed towards product, such process claim, which do not structurally distinguish the product, are given no patentable weight."

(Office Action, 03/09/06, p.3)

Applicants have amended claim 1 to include a substrate that has a first conductivity region and recesses, wherein the recesses have an inwardly concaved geometry with inflection points. A silicon or silicon alloy layer is deposited into the recesses to form a pair of inwardly concaved source/drain regions of a second conductivity type on opposite sides of the gate electrode.

It is respectfully submitted that Takeuchi'033 does not disclose, teach, or suggest such limitations of amended claim 1.

Takeuchi '033 discloses a MOS transistor. More specifically, as shown in Figure 1(h), Takeuchi'033 discloses a semiconductor substrate 101, a semiconductor layer 104 formed on substrate 101. Semiconductor layer 104 has the concentration of impurities higher than the concentration of impurities in substrate 101, and source and drain regions formed by a semiconductor layer 106 on semiconductor layer 104.

Takeuchi '033 addresses a punch-through phenomenon by forming a semiconductor layer between source/drain regions and a substrate that has the concentration of impurities higher than the concentration of impurities in the substrate.

Thus, Takeuchi'033 merely discloses a semiconductor substrate 101, and source and drain regions formed by layer 106 over semiconductor substrate, and does not disclose, teach, or suggest a substrate that has a first conductivity region and recesses, wherein the recesses have an inwardly concaved geometry with inflection points, as recited in amended claim 1. Furthermore, Takeuchi'033 does not disclose, teach, or suggest a silicon or silicon alloy layer deposited into the recesses to form a pair of inwardly concaved source/drain regions of a second conductivity type having a concentration of impurities in a range of $1x10^{18}/cm^3$ to $3x10^{21}/cm^3$ on opposite sides of the gate electrode creating metallurgical inflection points directly beneath the lower portion of the gate electrode formed directly on the gate dielectric layer, wherein the silicon or silicon alloy source/drain regions extend the greatest distance laterally beneath the lower portion of the gate electrode at the inflection points, which occurs between 50-250Å laterally beneath the gate electrode and at a depth of between 25-100Å beneath the gate dielectric, and directly define a first channel region having a first metallurgical channel length directly beneath the lower portion of the gate electrode in the first conductivity type region, and a second channel region having a second metallurgical length between the metallurgical inflection points, wherein the first

metallurgical channel length directly beneath the lower portion of the gate electrode is larger than the second metallurgical channel length between the metallurgical inflection points, as recited in amended claim 1.

Therefore, Applicants respectfully submit that amended claim 1 is not obvious under 35 U.S.C. § 103(a) over Takeuchi'033.

Because claims 8, 9, and 11 depend from amended claim 1, and add additional limitations, Applicants respectfully submit that claims 8, 9, and 11 are not obvious under 35 U.S.C. § 103(a) over Takeuchi'033.

Claim 3 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Takeuchi'033, in view of U.S. Patent No. 6,057,582 to Choi ("Choi '582").

Choi'582 discloses a transistor having a gate insulating film having thicknesses at both sides thicker than a thickness at a center formed on semiconductor substrate 21, and source/drain regions 27 formed in surfaces of the semiconductor substrate 21 on both sides of the gate electrode 23a (Figure 2, col. 3, lines 16-27).

It is respectfully submitted that Takeuchi'033 does not teach or suggest a combination with Choi'582, and Choi'582 does not teach or suggest a combination with Takeuchi'033. Takeuchi '033 teaches forming a semiconductor layer between source/drain regions and a substrate that has the concentration of impurities higher than the concentration of impurities in the substrate. Choi'582, in contrast, teaches the gate insulating film that is thicker at the sides than at the center. It would be impermissible hindsight based on Applicants' own disclosure, to combine Takeuchi'033 and Choi'582.

Furthermore, even if Takeuchi'033 and Choi'582 were combined, such a combination would lack the following limitations of amended claim 1: a substrate that has a first conductivity region and recesses, wherein the recesses have an inwardly concaved geometry

with inflection points. Additionally, a combination of Takeuchi'033 and Choi'582 would lack a silicon or silicon alloy layer deposited into the recesses to form a pair of inwardly concaved source/drain regions of a second conductivity type having a concentration of impurities in a range of $1x10^{18}/cm^3$ to $3x10^{21}/cm^3$ on opposite sides of the gate electrode creating metallurgical inflection points directly beneath the lower portion of the gate electrode formed directly on the gate dielectric layer, wherein the silicon or silicon alloy source/drain regions extend the greatest distance laterally beneath the lower portion of the gate electrode at the inflection points, which occurs between 50-250Å laterally beneath the gate electrode and at a depth of between 25-100Å beneath the gate dielectric, and directly define a first channel region having a first metallurgical channel length directly beneath the lower portion of the gate electrode in the first conductivity type region, and a second channel region having a second metallurgical length between the metallurgical inflection points, wherein the first metallurgical channel length directly beneath the lower portion of the gate electrode is larger than the second metallurgical channel length between the metallurgical inflection points, as recited in amended claim 1.

Because claim 3 contains discussed limitations, Applicants respectfully submit that claim 3 is not obvious under 35 U.S.C. § 103(a) over Takeuchi'033 in view of Choi'582. Claim 4 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Takeuchi '033 in view of U.S. Patent No. 5,970,351 to Takeuchi ("Takeuchi '351") as applied to claim 2 above, and in further view of Choi '582.

Takeuchi'351 discloses forming elevated source and drain regions formed on a substrate, and similarly to Takeuchi'033 and Choi'582, fails to disclose the discussed limitations of amended claim 1.

Because claim 4 depends from amended claim 1 and add additional limitations, Applicants respectfully submit that claim 4 is not obvious under 35 U.S.C. § 103(a) over Takeuchi'033, in view of Takeuchi'351, and further in view of Choi'582.

Claims 5 and 6 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Takeuchi '033 as applied to claims 1, 8, 9 and 11 above, and further in view of U.S. Patent No. 5,793,088 to Choi et al. ("Choi '088").

Choi'088 discloses controlling the threshold voltage by providing a threshold voltage implant into the edges of the halo regions, and similarly to Takeuchi'033 does not disclose the discussed limitations of amended claim 1.

Because claims 5 and 6 depend from amended claim 1 and add additional limitations, Applicants respectfully submit that claims 5 and 6 are not obvious under 35 U.S.C. § 103(a) over Takeuchi'033, in view of Choi'088.

Claim 12 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Takeuchi '033 as applied to claims 1, 8, 9 and 11 above, and further in view of U.S. Patent No. 5,567,966 to Hwang ("Hwang").

Hwang discloses thinning the channel region by local oxidation and wet etch, and similarly to Takeuchi'033, fails to disclose the discussed limitations of amended claim 1.

Because claim 12 depends from amended claim 1, Applicants respectfully submit that claim 12 is not obvious under 35 U.S.C. § 103(a) over Takeuchi'033, in view of Hwang.

Claim 13 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Takeuchi '033 in view of U.S. Patent No. 6,274,894 to Wieczorek et al. ("Wieczorek") in view of Takeuchi '351.

Wieczorek discloses forming low-bandgap source and drain regions for MOS transistors, and similarly to Takeuchi'033 and Takeuchi'351, fails to disclose the discussed limitations.

Because claim 13 contains the discussed limitations, Applicants respectfully submit that claim 13 is not obvious under 35 U.S.C. § 103(a) over Takeuchi'033, in view of Wieczorek, and further in view of Takeuchi'351.

Claim 14 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Takeuchi '033 in view of Wieczorek in view of Takeuchi '351 as applied to claim 13 above, and further in view of Choi '582.

As set forth above, neither Takeuchi'033, Wieczorek, Takeuchi'351, Choi'582, nor a combination thereof, discloses the discussed limitations.

Because claim 14 depends from amended claim 13, Applicants respectfully submit that claim 14 is not obvious under 35 U.S.C. § 103(a) over Takeuchi'033, in view of Wieczorek, in view of Takeuchi'351, and further in view of Choi'582.

Claim 15 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Takeuchi '033 in view of Wieczorek.

As set forth above, neither Takeuchi'033, Wieczorek, nor a combination thereof, discloses the discussed limitations.

Because amended claim 15 contains the discussed limitations, Applicants respectfully submit that amended claim 15 is not obvious under 35 U.S.C. § 103(a) over Takeuchi'033, in view of Wieczorek.

CONCLUSION

It is respectfully submitted that in view of the amendments and arguments set forth herein, the applicable rejections and objections have been overcome.

Pursuant to 37 C.F.R. 1.136(a)(3), applicant(s) hereby request and authorize the U.S. Patent and Trademark Office to (1) treat any concurrent or future reply that requires a petition for extension of time as incorporating a petition for extension of time for the appropriate length of time and (2) charge all required fees, including extension of time fees and fees under 37 C.F.R. 1.16 and 1.17, to Deposit Account No. 02-2666.

Respectfully submitted,

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Date: June 8, 2006

By: _____

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